6. The structure of claim 1 wherein said SiGe film is composed of two SiGe layers.

7. The structure of claim 1 further comprising a pMOS atop said SiGe film, said pMOS including a gate dielectric and an overlying gate conductor, said gate dielectric having a higher dielectric constant than SiO_2.

8. The structure of claim 7 wherein said gate dielectric is one of HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$ and Y_2O_3.

9. The structure of claim 7 wherein said gate conductor includes a p-type workfunction metal.

10. The structure of claim 7 further comprising an interfacial layer positioned between said semiconductor substrate and said gate dielectric.

11. The structure of claim 1 further comprising an oxide cap located atop said SiGe film.

12. The structure of claim 1 further comprising a silicon cap atop said SiGe film.

13. The structure of claim 12 wherein said silicon cap is amorphous, polycrystalline or single crystalline.

14. A structure including a SiGe engineered channel comprising:

a semiconductor substrate having at least one active area with an exposed upper surface of a semiconductor material of said semiconductor substrate, wherein isolation regions are present in said semiconductor material and are located at a periphery of said at least one active device region, each isolation region having an upper surface that is coplanar with the exposed upper surface of the semiconductor material;

a SiGe film located directly on the exposed upper surface of the semiconductor material active area, said SiGe film including a lower region that has a first Ge concentration and an upper region that has a second Ge concentration, wherein the first Ge concentration is greater than the second Ge concentration, and wherein said SiGe film has sidewall surfaces located above the isolation regions, wherein each sidewall surface of SiGe film is oriented perpendicular to a topmost surface of the semiconductor substrate and is vertically aligned to a sidewall edge of each isolation region that is located at the periphery of the at least one active device region; and

a p-type field effect transistor (pFET) located atop said SiGe film, said pFET comprising:

a gate dielectric and an overlying gate conductor, said gate dielectric having a higher dielectric constant than SiO_2, and

a source region and a drain region located within said SiGe film and extending into an upper portion of said semiconductor substrate, wherein a portion of said SiGe film located between said source region and said drain region is a channel region of said pFET.

15. The structure of claim 14 wherein said semiconductor substrate is a Si-containing semiconductor material.

16. The structure of claim 14 wherein said SiGe film includes a Si cap located atop an oxidized SiGe layer, said oxidized SiGe layer has a lower region and an upper region, wherein said lower region has a Ge concentration that is greater than 25 atomic percent and said upper region has a Ge concentration that is about 35 atomic percent or greater.

17. The structure of claim 16 wherein said Ge concentration in the lower region of said oxidized SiGe layer is about 30 atomic percent or greater and said Ge concentration in the upper region of said oxidized SiGe layer is about 35 atomic percent or greater.

18. The structure of claim 14 wherein said SiGe film is a graded SiGe layer.

19. The structure of claim 14 wherein said SiGe film is composed of two SiGe layers.

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